A CLASS OF MONOLITHIC HBT MULTIPLIERS

C.B. Perry, K.T. Ip, K.Z. Claxton, B.R. Allen, A.E. Farris

TRW Inc.
One Space Park, Redondo Beach, CA. 90278

Abstract

Two types of monolithic multipliers have been developed using current AlGaAs HBT technology. Both circuits have an intended input frequency range of 10 MHz to 1.0 GHz. Preliminary wafer probe measurements indicate the even order multiplier achieves 45 dB of fundamental rejection and 22 dB conversion loss at 2.5 GHz (10th harmonic), consuming 175 mW. The odd order multiplier exhibited 21 dB of conversion loss at 10 GHz (10th harmonic) and 35 dB at 21 GHz (21st harmonic), dissipating 315 mW. These circuits offer significant improvement in bandwidth, output power and lower implementation cost compared to existing diode-based MIC or MMIC MESFET frequency multipliers.

Introduction

Frequency multipliers are often realized using SRD diodes in a MIC configuration. These circuits have narrow bandwidth , require tuning and high RF drive levels (> 10 dBm) to generate high harmonics. Frequency multipliers have also been realized in MMIC form using GaAs MESFET technology. However, device limitations restrict MESFET frequency multiplication to the second or third harmonic region [1]. The AlGaAs HBT device technology offers potential for improved performance in this application. HBT devices have been shown to exhibit higher efficiency, lower phase noise and superior device uniformity compared to MESFET and HEMT devices [2] . The HBT's inherent high f_T and bipolar structure permits the design of analog circuits in MMIC form that operate into the microwave region.

This paper reports on the modelling, design, and performance of two monolithic HBT frequency multipliers. The multipliers are designed to operate over a 3 decade input bandwidth, generating high-order harmonics while requiring minimal RF input drive and DC power. An analog design approach was chosen in preference to a distributed methodology. The analog approach circumvents the requirements of using large quarter-wave structures and enables frequency multiplication into the low megahertz region. The multipliers are designed with on-chip temperature and current gain compensation networks to ensure operation over environmental and process variations. The circuits were fabricated using 3 µm emitter, self aligned base ohmic metal process and molecular beam epitaxy growth described previously [2]. Each circuit requires one -5 VDC supply and measures 2.5 x 1.25 mm^2. The circuits were designed and analyzed using EEsof's Microwave Spice simulation software.

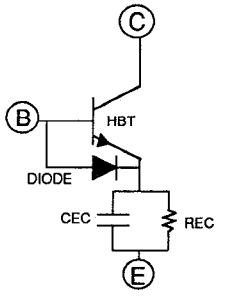
HBT Device Model

A HBT device model was developed to predict frequency response and harmonic output power of the even and odd multiplier circuits. The HBT device operates both as a linear and non-linear element throughout the circuit, and it is therefore important to develop both large and small signal models. Initially, a large signal model is developed using measured I-V data and knowledge about the device's construction and geometry. Once the large signal model is determined, it is used to generate small signal (linear) s-parameters. The model-generated s-parameters are then compared to measured s-parameters of identical devices.

If error exists between the measured and modelled s-parameters, the RF parameters of the large signal model are varied until a satisfactory fit is achieved. The goal is to develop a large signal model that will generate small signal s-parameters when excited linearly. This enables prediction of output power level as well as linear frequency response with one device model.

The large signal SPICE model shown in Figure 1, utilizes a modified Gummel-Poon model previously described [3]. This model is compatible with EEsof's Microwave Spice software and consists of a NPN HBT device and diode connected across the base-emitter junction. The diode simulates the surface re-combination effects in the base-emitter junction and emitter resistance (REC) and capacitance (CEC) parameters are modelled as a parallel R-C network outside the transistor structure. The HBT's emitter resistance and capacitance, as well as internal base resistance and built-in potential are process dependent variables that effect RF performance. These parameters are adjusted until the model generated s-parameters match s-parameters of a recently measured device. Measured s-parameter data should be selected form various wafers after the most recent process to insure a current and balanced parameter characterization.

Single emitter, 3 X 10 µm devices were used in the signal path due to the small emitter capacitance and high frequency capability. Dual and quad emitter, 3 X 10 µm devices were used as current references and level shifters in the circuit.



HBT:

IS=	1.16E-24 A	ISE=	2.2E-23 A
ISC=	4.09E-14 A	BF=	1E5
BR=	.01	VAF=	800 V
VAR=	700 V	KF=	3.2E-13
NE=	1.3	NF=	1.11
NR=	1.0	NC=	2.0
RB=	47 Ω	RC=	15 Ω
CJE=	45 fF	VJE=	1.45 V
MJE=	0	TF=	6.1 pS
PTF=	38.2	CJC=	46 fF
VJC=	1.21 V	MJC=	.5
XCJC=	.34	FC=	.69
CJS=	35 fF		

DIODE:

IS=	7.56E-18 A
KF=	1.6E-13
N=	2.06

REC= 14 Ω
CEC= .25pF

Figure 1. Large Signal 3 x 10 μm^2 Spice Model

Multiplier Circuit Design

The even order multiplier is designed to provide even order multiples of the input frequency, while suppressing the fundamental and all odd harmonic tones. The circuit consists of an input differential amplifier chain which amplifies and limits the input sinusoid. Complementary square waves at the chain outputs are injected into a single time constant network, producing complementary pulse trains. The complimentary pulse trains are then amplified and combined, producing an even harmonic output spectra. Figure 2 illustrates the circuit block diagram.

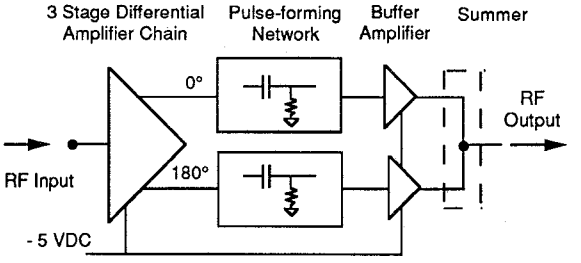


Figure 2. Even Order Multiplier Block Diagram

The odd order multiplier is constructed using the even circuit approach, except in the output stage. Due to the odd harmonic nature of the complementary pulse trains, a differential pair is used as an output amplifier and buffer stage. A 3 dB improvement in output power can be achieved by implementing an off-chip 180° hybrid at the output ports. Figure 3 illustrates the circuit block diagram.

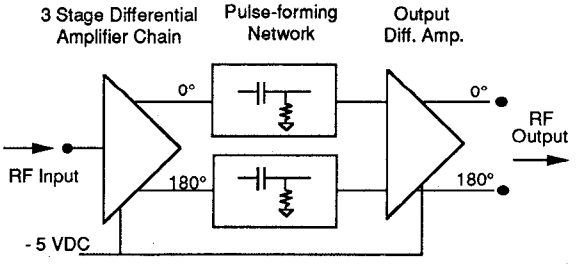


Figure 3. Odd Order Multiplier Block Diagram

Temperature and process variation was also considered. The multipliers utilize a bias adjustment network which regulates current supplied to the differential chain. This network can be adjusted to supply additional current in the differential stages for low ß circuits. Higher current flow ensures waveform saturation and square wave outputs at the third differential stage. Diodes connected across the base of the bias network provide stable current flow over temperature. Both circuits are designed with 50 ohm, single-ended input ports for good input match, and emitter follower stages between differential pairs to reduce loading and extend operating bandwidth. Figure 4 illustrate the even order circuit schematic. Both even and odd order MMIC multipliers measure 1.25 x 2.5 mm^2 and are shown in Figures 5 and 6 respectively.

Even Order Multiplier Performance

The even order multiplier was tested with input frequencies of 250 MHz and 1.0 GHz at -10 dBm. RF yield averaged 72%. The circuit was tested on-wafer, using a HP 8340B signal synthesizer and HP 8566B spectrum analyzer. The multiplier was biased at -5 VDC and required 35 mA.

Measured performance in Figure 7 indicates at 250 MHz and -10 dBm input conditions, the even order multiplier exhibited 22 dB conversion loss at the 10th harmonic. Odd harmonic rejection measured greater than 40 dB to the 9th harmonic. Even harmonic conversion loss ranged from 10 to 22 dB to 2.5 GHz.

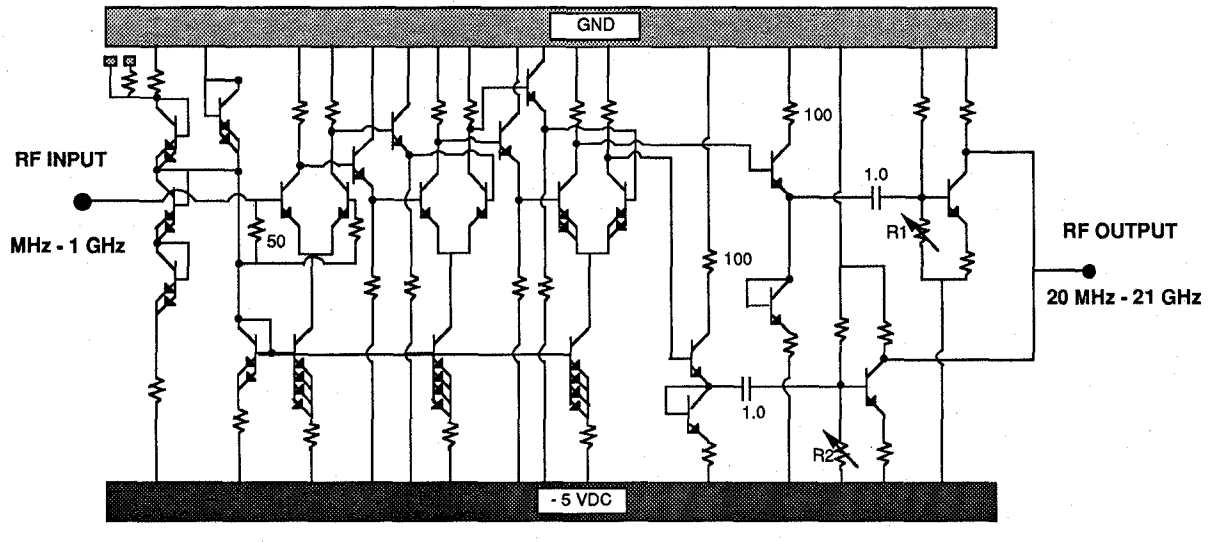


Figure 4. Even Order Circuit Schematic

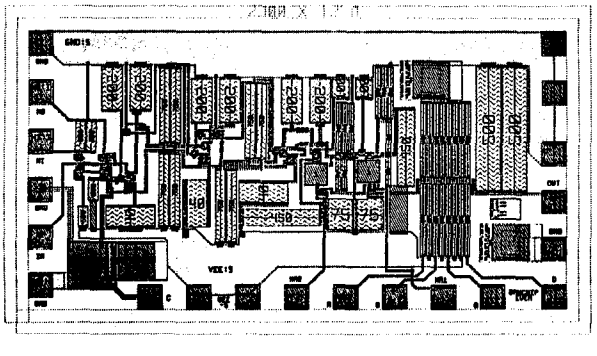


Figure 5. Even Order HBT MMIC Circuit

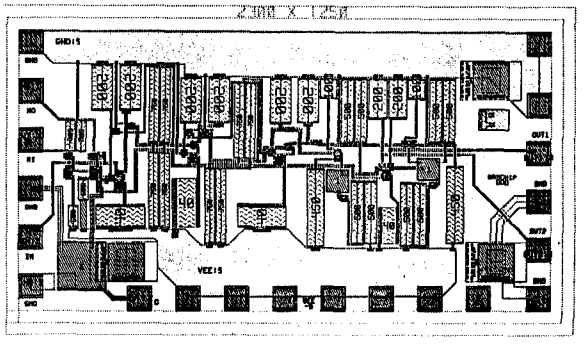


Figure 6. Odd Order HBT MMIC Circuit

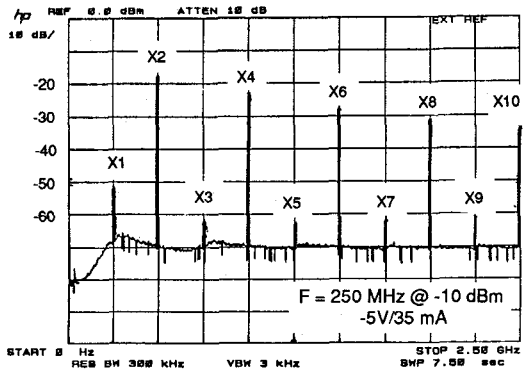


Figure 7. Even MMIC Output Spectrum to 2.5 GHz

Figure 8 illustrates measured performance at 1GHz and -10 dBm. The even order multiplier exhibited 20 dB conversion loss at 4 GHz and 40 dB odd harmonic rejection at 5 GHz. Conversion loss and rejection begins to degrade in the 8 GHz region primarily due to device and circuit path asymmetries.

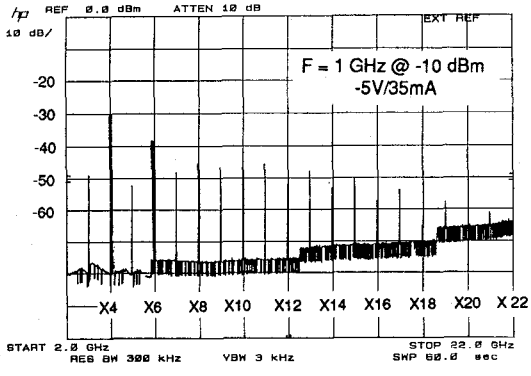


Figure 8. Even MMIC Output Spectrum to 22 GHz

Odd Order Multiplier Performance

The odd order multiplier was tested using identical conditions and equipment as the even order multiplier. The multiplier was biased at -5 VDC and 63 mA. RF yield averaged 65%. At 250 MHz and -10 dBm, the multiplier exhibited 14 dB conversion loss at the 10th harmonic. Even harmonic rejection measured 18 dB to 2.5 GHz (Fig. 9). Measured performance at 1 GHz and -10 dBm indicated 35 dB conversion loss at 21 GHz. Odd harmonic output power is greater than -35 dBm to 15 GHz with even harmonic rejection ranging form 20 to 30 dB (Fig 10).

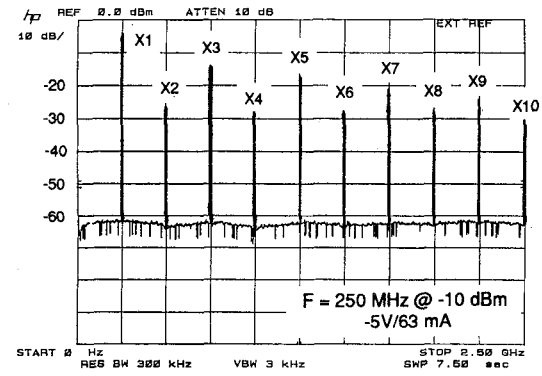


Figure 9. Odd MMIC Output Spectrum to 2.5 GHz

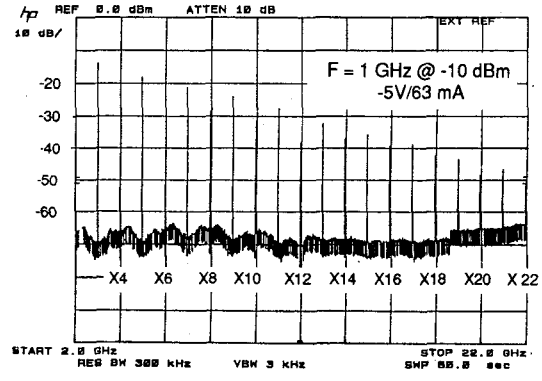


Figure 10. Odd MMIC Output Spectrum to 22 GHz

Conclusion

Two types of monolithic HBT frequency multipliers have been developed. Measurements indicate frequency multiplication at the 21st harmonic (21 GHz) can be achieved with 35 dB conversion loss. Additionally, 40 dB of adjacent harmonic rejection is also reported. Monolithic HBT multipliers generate high harmonic frequencies as do the SRD multipliers, but exhibit wider bandwidth and higher output power using lower RF input drive. The described multipliers exhibit adjacent harmonic rejection which can be useful in relaxing external filter requirements. Finally, monolithic design eliminates tuning which ensures stability and reduces the cost of circuit integration.

[1] S.A. Maas, Nonlinear Microwave Circuits, Artech House, Dedham, 1987, pp 398-404.
[2] B. L. Nelson, C.B. Perry, et al., "High Linearity,Low DC Power HBT Broadband Amplifiers to 11 GHz," in 1989, IEEE GaAs IC Symp. Dig. (San Diego) Oct. 1989, pp. 79-82
[3] C. P. Grossman, A. Oki, "A Large Signal DC Model for GaAs Heterojunction Bipolar Transistors," Proc. of the IEEE Bipolar Circuits and Tech. Meeting, Sept. 1989, pp 258-262